CLAIM AMENDMENTS

Please amend the claims as follows:

1. (Currently Amended) A method for demodulation of a ~~composite~~ signal containing a plurality of multi-path components, the method comprising:

buffering digital samples of [[a]] the signal into a first memory element, wherein a set of the digital samples represents a first symbol group corresponding to a first symbol;

randomly accessing the digital samples from the first memory element;

serially determining a channel estimate for each of a plurality of different multi-paths to generate a plurality of channel estimates;

selecting, based on instantaneous powers of the plurality of channel estimates, a set of relevant multi-paths that includes a subset of the plurality of different multi-paths;

performing an iterative process to determine a symbol estimate that is stored in a second memory element, wherein the iterative process includes, for each multi-path of the set of relevant multi-paths,

extracting a multi-path component for a particular multi-path,

multiplying the multi-path component with a channel estimate for the particular multi-path to generate an intermediate symbol estimate, and

accumulating the intermediate symbol estimate into the symbol estimate

~~to correlate a particular multi-path component from the signal; and~~

~~iteratively accumulating the correlated particular multi-path component into a second memory element.~~

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Currently Amended) The method of claim 1, further comprising performing channel estimation and demodulation via ~~the~~ non-sequential access of digital samples from the first memory element.

6. (Previously Presented) The method of claim 1, further comprising:

tuning to a non-original RF frequency;

buffering digital samples obtained while tuned at the non-original RF frequency in the first memory element;

retuning the RF frequency to an original frequency; and

performing searching and channel estimation via the random access of the digital samples stored in the first memory element while simultaneously operating on the digital samples of the original frequency.

7. (Currently Amended) An apparatus configured to demodulate a ~~composite~~ signal containing a plurality of multi-path components, the apparatus comprising:

a plurality of buffers configured to receive and store chip samples from a receiver ~~be switchable between a write state with digital samples and a read state by a correlating element~~; and

~~a despreading element that operates via random access of buffers that are currently in read state to accumulate energy for a particular multi-path component;~~

~~a weighting element that weights despread energy for a particular multi-path component using a channel estimate of the particular multi-path component; and~~

~~an accumulator that iteratively accumulates the weighted despread energy for each particular multi-path component~~

a processor, operatively coupled to the plurality of buffers, and adapted to access, from the plurality of buffers, a first block of the chip samples corresponding to a first symbol group, and to perform an iterative process of serially extracting, from the first block, a multi-path component for each of a plurality of multi-paths in order to produce a plurality of extracted multi-path components, to multiply the plurality of extracted multi-path components with a plurality of channel estimates, and to accumulate results into a symbol buffer,

wherein the apparatus is adapted to transition the processor into a sleep mode after the processor has completed the iterative process for the first block of chip samples, and to transition the processor into a processing mode when a second block of chip samples corresponding to a second symbol group is available to be processed.

8. (Cancelled)

9. (Currently Amended) The apparatus of claim 7, wherein the plurality of buffers is comprised of three ~~physically~~ separate buffers such that at any given time, one of the three ~~physically~~ separate buffers is receiving data, and two of the three ~~physically~~ separate buffers comprise a logical buffer for random access by the processor ~~a correlator~~.

10. (Currently Amended) The apparatus of claim 7, wherein the plurality of buffers is comprised of five ~~physically~~ separate buffers such that at any given time, two of the five ~~physically~~ separate buffers comprise a logical data source ~~logically addressable space~~ that is receiving data, and the other three of the five ~~physically~~ separate buffers comprise a logical data source ~~logically addressable space~~ for random access by the processor ~~a correlator~~.

11. (Cancelled)

12. (Currently Amended) The apparatus of claim 7, ~~further comprising circuitry to~~ wherein the processor is adapted to perform searches for multi-path components by correlating the components ~~against a timing hypothesis~~.

13. (Currently Amended) The apparatus of claim 7, ~~further comprising a permutation block following a plurality of physical buffers,~~

wherein the plurality of buffers comprises ~~separate sets of physical buffers~~ a first buffer for even phase samples and a second buffer for odd phase ~~digital~~ samples, and

wherein the ~~permutation~~ processor is further adapted to implement a permute block, which supplies samples stored in the first buffer ~~is capable of mapping to one set of the separate sets of physical buffers~~ to ~~the~~ a searching ~~element~~ function of the processor, and ~~one set of the separate sets of physical buffers~~ the permute block supplies samples stored in the second buffer to ~~the~~ a demodulation ~~element~~ function of the processor, whereby the ~~permutation~~ permute block manages contention between the searching ~~element~~ function and the demodulation ~~element~~ function for access to ~~data in~~ a same memory block.

14. (Cancelled)

15. (Previously Presented) The apparatus of claim 7, further comprising:

means for tuning to a non-original RF frequency;

means for buffering digital samples obtained while tuned at the non-original RF frequency in a first memory element;

means for retuning the RF frequency to the original frequency; and

means for performing searching and channel estimation via the random access of the digital samples stored in the first memory element while simultaneously operating on the digital samples of the original frequency.

16. (Original) The apparatus of claim 15, wherein the means for buffering digital samples obtained while tuned at the non-original RF frequency maintains digital samples from the non-original RF frequency after retuning the RF frequency to the original frequency.

17. (Original) The apparatus of claim 7, further comprising means for processing a plurality of sets of digital samples from a plurality of distinct receiver RF chains.

18. (Original) The apparatus of claim 7, further comprising means for processing multi-path components corresponding to transmit diversity.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (Cancelled)

26. (Currently Amended) The apparatus of claim 7 ~~demodulator of claim 20~~, wherein the chip samples correspond to ~~digital samples obtained from the first memory buffer include~~ a burst-pilot signal transmitted by a base-station ~~that is time-division multiplexed, wherein the burst-pilot signal includes information relating to a cellular channel used to determine the channel estimate~~.

27. (Currently Amended) The apparatus of claim 7 ~~demodulator of claim 20~~, wherein the chip samples correspond to ~~digital samples obtained from the first memory buffer include~~ a continuous-pilot signal transmitted by a base-station~~, wherein the continuous-pilot signal includes information relating to a cellular channel used to determine the channel estimate~~.

28. (Currently Amended) The apparatus of claim 7 ~~demodulator of claim 20~~, wherein the ~~digital~~ chip samples ~~obtained from the first memory buffer~~ include samples that correspond

to signals communicated in a multiple input ~~transmit~~, multiple output ~~receive~~ antenna scheme.

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (New) The method of claim 1, wherein selecting the set of relevant multi-paths comprises:

determining, from the instantaneous powers, a strongest instantaneous power; and

excluding, from the set, each of the different multi-paths that have an instantaneous power that is greater than a threshold value below the strongest instantaneous power.

35. (New) The method of claim 1, wherein selecting the set of relevant multi-paths comprises:

excluding, from the set, each of the different multi-paths that have an instantaneous power that is below a threshold value.

36. (New) The apparatus of claim 7, wherein the processor is further adapted:

to serially determine a channel estimate for each of the plurality of multi-paths to generate the plurality of channel estimates; and

to select, based on instantaneous powers of the plurality of channel estimates, a set of relevant multi-paths that includes a subset of the plurality of multi-paths, and

wherein performing the iterative process includes, for each multi-path of the set of relevant multi-paths,

extracting a multi-path component for a particular multi-path,

multiplying the multi-path component with a channel estimate for the particular multi-path to generate an intermediate symbol estimate, and

accumulating the intermediate symbol estimate into the symbol buffer.

37. (New) A method for demodulation of a signal containing a plurality of multi-path components, the method comprising:

buffering digital samples of the signal into a first memory element, wherein a set of the digital samples represents a first symbol group corresponding to a first symbol;

when a set of the digital samples corresponding to a first symbol group is available, activating a processor to generate a first symbol estimate for the first symbol group, wherein generating the symbol estimate includes

serially determining a channel estimate for each of a plurality of different multi-paths to generate a plurality of channel estimates;

selecting, based on instantaneous powers of the plurality of channel estimates, a set of relevant multi-paths that includes a subset of the plurality of different multi-paths;

performing an iterative process to determine the first symbol estimate that is stored in a second memory element, wherein the iterative process includes, for each multi-path of the set of relevant multi-paths,

extracting a multi-path component for a particular multi-path,

multiplying the multi-path component with a channel estimate for the particular multi-path to generate an intermediate symbol estimate, and

accumulating the intermediate symbol estimate into the first symbol estimate;

deactivating the processor when the iterative process is completed; and

when a set of the digital samples corresponding to a second symbol group is available, again activating the processor to generate a second symbol estimate for the second symbol group.

38. (New) The method of claim 37, wherein selecting the set of relevant multi-paths comprises:

determining, from the instantaneous powers, a strongest instantaneous power; and

excluding, from the set, each of the different multi-paths that have an instantaneous power that is greater than a threshold value below the strongest instantaneous power.

39. (New) The method of claim 37, wherein selecting the set of relevant multi-paths comprises:

excluding, from the set, each of the different multi-paths that have an instantaneous power that is below a threshold value.